OCT 0 2 2000 Docket No.: Z&PINFP08190 COT - 1.

Thereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231, on the date indicated below.

By: M. P.

Date: September 28, 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants

Giuseppe Curello et al.

Applic. No.

09/904,360

Filed

July 12, 2001

Title

Process for Producing a Doped Semiconductor Substrate

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks, Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

U. S. Patent 5,989,963 (Luning et al.) dated November 23, 1999;

U. S. Patent 5,963,801 (Aronowitz et al.) dated October 5, 1999;

Noda et al.: "0.1 µm Delta-doped MOSFET using Post Low-energy Implanting Selective Epitaxy" 1994 Symposium on VLSI Technology Digest of Technical Papers, pages 19 – 20;

Priolo et al.: "Interface evolution and epitaxial realignment in polycrystal/single crystal Si structures" 1994 Elsevier Science B.V. 1994, Nuclear Instruments and Methods in Physics Research B85, pages 159 – 166;

Transactions on Electron Devices, Vol. 39, No. 7, July 1992, pages 1704 – 1711;

Thompson et al.: "MOS Scaling: Transistor Challenges for the 21st Century" Intel Technology Journal Q3'98, pages 1 – 19;

Curello et al.: "Beam-power heating effect on the synthesis of graded composition epitaxial Si_{1-x}Ge_x alloy layers" Elsevier Science B.V., 1997, Nuclear Instruments and Methods in Physics Research B 129, pages 377 - 386.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the Applicants.

Respectfully submitted,

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